

## Abstract of the Disclosure

The preferred embodiments described herein provide a memory device and method for redundancy/self-repair. In one preferred embodiment, a memory device is provided comprising a primary block of memory cells and a redundant block of memory cells. In response to an error in writing to the primary block, a flag is stored in a set of memory cells allocated to the primary block, and the redundant block is written into. In another preferred embodiment, an error in writing to a primary block is detected while an attempt is made to write to that block. In response to the error, the redundant block is written into. In yet another preferred embodiment, a memory device is provided comprising a three-dimensional memory array and redundancy circuitry. In still another preferred embodiment, a method for testing a memory array is provided. Other preferred embodiments are provided, and each of the preferred embodiments described herein can be used alone or in combination with one another.

10  
To the reader of this document